

Controlled Impedance Note — RO4350B (h = 0.102 mm)

Stackup Details

- Material: Rogers RO4350B
- Dielectric constant (Design Dk): 3.66 (diff-phase method)
- Dielectric constant (Process Dk): 3.48 ± 0.05 (IPC clamped)
- Dielectric thickness (h): **0.102 mm**
- Copper thickness: 35 μm base, ~40–45 μm finished after plating
- Solder mask: None (maskless RF traces over air)
- Reference: Continuous ground plane directly beneath RF layer

Targets

Differential pair (LVDS)	$Z_{\text{diff}} = 100\ \Omega \pm 8\%$
Single-ended reference	$Z_0 = 50\ \Omega \pm 10\%$

Starting Geometry (maskless microstrip)

Values are starting points for PCBWay CAM to field-solve and tune with coupons.

Assumption	50 Ω microstrip (w, mm)	100 Ω diff pair (w, mm)	100 Ω diff pair (s edge-edge, mm)
Process Dk = 3.48	0.204	0.204	0.26
Design Dk = 3.66	0.195	0.195	0.26

Alternate Option (keep w = 0.204 mm; adjust gap for Design Dk)

Assumption	w (mm)	s edge-edge (mm)	Expected Z_{diff}
Design Dk = 3.66	0.204	0.30	$\approx 100\text{--}102\ \Omega$

Routing Rules

- Continuous reference plane; no splits/slots beneath the pair
- Point-to-point routing; no stubs or tees; equal via count per leg
- Intra-pair length match: $\leq 1\text{--}2\ \text{mm}$ for 10.5 GHz RF; $\leq 5\ \text{mm}$ for LVDS clocks
- No same-layer ground pour near the pair unless re-solved for CPWG
- If via fencing is used: via-center to outer trace edge $\approx 0.5\ \text{mm}$; pitch $\leq 1.0\ \text{mm}$; symmetric on both sides
- Receiver termination: 100 Ω differential (omit external if receiver provides internal 100 Ω)

Coupon/Test Notes

- Provide impedance coupons for both 50 Ω microstrip and 100 Ω differential pair
- PCBWay may tune w by $\pm 0.02\text{--}0.04\ \text{mm}$ and/or s by $\pm 0.03\text{--}0.05\ \text{mm}$ to hit targets
- Return as-built geometry values (w, s) in the fab report